REMARKS

Reconsideration and allowance are requested.

Applicants request acknowledgement of the foreign priority claim and receipt of the certified copy of the priority document.

An information disclosure statement is submitted bringing to the attention of the Examiner a copy of the International Preliminary Examination Report in the corresponding PCT application. Consideration is requested.

Multiple claims stand rejected for anticipation under 35 U.S.C. §102 based on Grochoski (US-B-6,353,883). This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Grochoski fails to satisfy this rigorous standard.

Grochoski discloses predicting predicate values which will be resolved for predicated instructions. The Examiner argues that Grochoski discloses a predication instruction. Applicants disagree. Grochoski's predicated instruction is a conditional instruction such as IF...THEN..., and a predicate value is a condition code. But neither is a predication instruction as recited in claims 1 and 18. Those claims both specify that execution of the claimed predication instruction controls "execution of one or more associated instructions in dependence upon one or

more condition states [e.g., condition codes] of said apparatus for processing data set by execution of one or more program instructions **other than** said predication instruction."

The Examiner's contention that a predicated instruction, such as IF (p2) THEN MOVE 6, is the claimed predication instruction does not withstand scrutiny. Grochoski's IF-THEN instruction is a conditional instruction in itself that does not control the execution of other instructions. For example, Grochoski's COMPARE instruction sets the condition codes itself and so cannot be the predication instruction recited in claims 1 and 18.

In addition, amended claim 1 incorporates the features of claims 12-15 and claim 18 the features of claims 29-32. These dependent claim features are admitted as lacking from Grochoski. To supply one of those missing features, the Examiner turns to US-B-6,910,123 to Bosshart. Applicants respectfully traverse this obviousness rejection based on Grochoski and Bosshart.

Bosshart does not teach "a predicated instruction counter register operable to store a counter value indicative of *how many of said one or more associated program instructions subject to said predication instruction have been executed.*" Referring to the column 23, line 1 through column 24, line 65 relied by the Examiner, the counters AO and Al count iterations of groups of instructions rather than how many of the predicated instructions subject to a predication instruction have been executed, as is specified in amended claims 1 and 18.

The Examiner further admits that Grochowski lacks "an exception handling circuit operable upon occurrence of an exception to store said counter value and upon completion of said exception to restart execution starting at a program instruction pointed to by said counter value," as quoted from amended claim 1. The Examiner suggests this feature is taught in US-B-6,886,094 Blandy. Applicants respectfully disagree.

Blandy is generally concerned with exception handling within a virtual machine system that uses "just-in-time" compilation. Although columns 8, 9 and 10 of Blandy referred to by the Examiner describe exception handling within a virtual machine, there is no description of storing the claimed counter value upon occurrence of an exception and using that counter value as the point for restarting execution upon completion of the exception.

So the independent claims recite multiple features not taught by Grochowski alone or in combination with Bosshart or Blandy. Moreover, the combination of features recited in claims 1 and 18 provides advantages that are not achieved by the applied prior art. A program counter register and a predicated instruction counter register are operated in conjunction with the exception handler to allows interruption of predicated instruction sequences and a return after interrupt in a way that keeps interrupt latency low. Although it might be simple and superficially attractive approach to treat a predication instruction and the instruction(s) it predicates as an atomic entity which cannot be interrupted partway through, such an approach substantially increases interrupt latency. That kind of interrupt latency increase is unacceptable in many real time processing situations and in general.

None of the prior art documents discloses or suggests the above features or addresses the issue of increased interrupt latency associated with predication instructions. But the inventors recognized this problem and avoided it by providing a predicated instruction counter register to store a counter value indicating the number of predicated instructions executed at the point of interrupt. Then when a return from an interrupt is made, the predication instruction can be identified using the program counter, and the point within the predicated instruction sequence reached can be identified by the counter value.

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

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